REMARKS

The Final Office Action mailed July 29, 2002, has been received and reviewed. claims 1 through 20 are currently pending in the application. claims 1 through 20 stand rejected. Applicants propose to amend claims 1, 10 and 20, cancel claims 2, 3, 11 and 12, and thus respectfully request reconsideration of the application as proposed to be amended herein.

Claims 1 and 10 have been amended to include an insulating layer of doped BPSG. The claims thus include an interface between the BPSG and dielectric layers. Such an interface is necessary in order for the benefits of the invention to be realized. Furthermore, in order to underscore the function of the TEOS layer as 1) a barrier to dopant diffusion between the BPSG layer and the dielectric layer, and 2) a measure for reducing build up of dopant along layer interfaces, claims 1 and 10 now refer to a TEOS layer which is "substantially dopant-free."

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on U.S. Patent No. 6,274,423 to Prall et al. in View of U.S. Patent No. 6,124,626 to Sandhu et al.

Claims 1 through 4, 6 through 15, and 17 through 20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Prall et al. (U.S. Patent No. 6,274,423) in view of Sandhu et al. (U.S. Patent No. 6,124,626). Applicants respectfully traverse this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

Applicant respectfully submits that the Examiner fails to establish a *prima facie* case of obviousness.

First, the combination of Prall and Sandhu fails to teach every element of Applicants' claims as amended.

Prall teaches an interface between the dielectric layer and the overlying, insulating BPSG layer. As Applicants teach in paragraph [004] of the specification, such an interface is susceptible to degradation during wet etch steps subsequent to the formation of the interface. The degradation susceptibility is due to high concentrations of dopant at the interface. Prall merely teaches the state of the art in the absence of Applicants' device, as disclosed in Applicants' specification.

Sandhu teaches the use of *ozone enhanced* materials as the first electrode or as a layer overlying the capacitor structure. Col 6, lines 43-44, Col 5, lines 34-37. With respect to the use of TEOS as an overlayer, Sandhu only teaches the use of ozone enhanced TEOS. Sandhu cannot be read to teach the use of substantially dopant-free TEOS because the incorporation of ozone is required by Sandhu to prevent the loss of oxygen in the dielectric, and, thus, loss of capacitor performance, due to the process of depositing post-capacitor layers. In contrast, Applicants' device requires a substantially dopant-free TEOS layer in order to function as a dopant barrier (specification, paragraph [0042]) between the BPSG and dielectric layers. An appreciably doped TEOS layer would tend to increase the amount of dopant build-up and dopant diffusion at the border shared by the cell nitride layer and the TEOS layer. Such a build-up would render the border susceptible to damage by the etch process associated with the deposition of post-capacitor layers, the very problem that Applicants' invention addresses. Thus, the combination of Prall and Sandhu does not teach every element of Applicants' claims.

Furthermore, there is no suggestion or motivation in either reference to modify the device of Prall with the teachings of Sandhu to arrive at Applicants' invention. Prall does not suggest the existence of or attempt to solve the problem that is addressed by Applicants' invention,

namely interface degradation. Instead, the process of Prall is directed toward a process for improved isolation of bit line contacts from other capacitor components.

Sandhu, like Prall, does not contain the motivation or suggestion to combine. Sandhu does disclose "a TEOS layer disposed between the BPSG layer and the capacitor structure to wrap around difficult edges or plates" (albeit ozone enhanced, thus doping is permissible). From the above, the Examiner concludes that "it would have been obvious to one "skilled in the art" to use the TEOS layer disposed between the BPSG layer and the capacitor structure into the Prall et al. device to wrap around difficult edges, plates and provide dielectric oxygen loss protection."

However, like Prall, Sandhu does not in any way suggest the insertion of a TEOS-overlaid capacitor structure for the capacitor structure of Prall. As with Prall, Sandhu does not mention or suggest the interface degradation problem addressed by Applicants' device. Sandhu's teachings pertain to oxygen loss in a dielectric, not interface degradation.

Furthermore, the words "to wrap around difficult edges, plates. etc." cannot be taken as a suggestion that the silicon layer of Sandhu "encase" the dielectric and cellplate end portions as required by Applicants' claims. Col 6, lines 45-50, *See* claims 1 ands 10. It must be noted that the "edge" (55) referred to is nothing like the "ends" referred to in Applicants' claims, for it refers to the edge of lower electrode (52), not the edge of the upper electrode or the edge of the dielectric, which, after wrapping over electrode edge (52), extends away from it. *See* Fig. 2. Thus, wrapping of the "difficult edge" referred to in Sandhu is not at all the encasing of upper electrode and dielectric end portions recited by Applicant's claims.

Moreover, even if the knowledge available to one skilled in the art motivated one to combine teachings, every element of Applicants' claims is not met. Applicants' device requires substantially dopant-free TEOS in order to fulfill its function as a dopant barrier (specification, paragraph [0042]), whereas the combination of prior art yields a device which requires ozone enhanced TEOS.

Applicants thus respectfully submit that neither Prall nor Sandhu nor the knowledge available to one skilled in the art suggests or motivates the combination of Prall with Sandhu.

Claims 1 and 10 are therefore in condition for allowance. Furthermore, claims 4-9, and 13-20 are deemed allowable as dependent from allowable independent claims.

Obviousness Rejection Based on U.S. Patent No. 6,274,423 to Prall et al. and U.S. Patent No. 6,124,626 to Sandhu et al. and Further in View of U.S. Patent No. 5,763,306 to Tsai

Claims 5 and 16 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Prall et al. (U.S. Patent No. 6,274,423) and Sandhu et al. (U.S. Patent No. 6,124,626), as applied to claims 1 through 4, 6 through 15, and 17 through 20 above, and further in view of Tsai (U.S. Patent No. 5,763,306). Applicants respectfully traverse this rejection, as claims 5 and 16 are both depending from allowable independent claims.

ENTRY OF AMENDMENTS

The proposed amendments to claims 1 and 10 above should be entered by the Examiner because the amendments are supported by the as-filed specification and drawings and do not add any new matter to the application. Further, the amendments do not raise new issues or require a further search. Finally, if the Examiner determines that the amendments do not place the application in condition for allowance, entry is respectfully requested upon filing of a Notice of Appeal herein.

CONCLUSION

Claims 1, 4 through 10 and 13 through 20 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicants' undersigned attorney.

Respectfully Submitted,

Joseph A. Walkowski
Registration Number 28,765
Attorney for Applicant
TRASKBRITT, PC
P.O. Box 2550
Salt Lake City, Utah 84110
Telephone: (801) 532-1922

Date: October 1, 2002
JAW/ps:dlm
Enclosure: Version With Markings to Show Changes Made

N:\2269\4475.1\Amendment Final.wpd

VERSION WITH MARKINGS TO SHOW CHANGES MADE

1. (Amended) A DRAM circuit comprising:

a substrate having a capacitor structure disposed thereon, said capacitor structure including a storage node, a dielectric layer overlying said storage node, and a conductive cell plate overlying said dielectric layer, each of said dielectric layer and said conductive cell plate having an end portion;

a conductive contact extending downward and adjacently beside said capacitor structure, said end portion of said dielectric layer extending closer to said conductive contact than said end portion of said conductive cell plate; [and]

a substantially dopant-free TEOS layer disposed over said capacitor structure and encasing said end portions of said dielectric layer and said conductive cell plate, said TEOS layer disposed between said capacitor structure and said conductive contact; and

a doped BPSG layer disposed over said TEOS layer, said conductive contact extending through said BPSG layer and said TEOS layer.

10. (Twice Amended) A semiconductor memory device comprising:

a semiconductor substrate having a capacitor structure formed thereon, said capacitor structure including a first conductive layer, a second conductive layer, and a dielectric layer, said dielectric layer disposed between said first and second conductive layers, each of said dielectric layer and said first and second conductive layers having an end portion;

a conductive contact extending downward and adjacently beside said capacitor structure, said end portion of said dielectric layer extending closer to said conductive contact than said end portion of each of said first conductive layer and said second conductive layer; [and]

a substantially dopant-free TEOS layer disposed over said capacitor structure and encasing said end portions of said dielectric layer and each of said first conductive layer and said second conductive layer, said TEOS layer disposed between said capacitor structure and said conductive contact; and

a doped BPSG layer disposed over said TEOS layer, said conductive contact extending through said BPSG layer and said TEOS layer.

20. (Twice Amended) The device of claim [11]10, wherein said TEOS layer comprises a dopant barrier between said capacitor structure and said insulating layer.